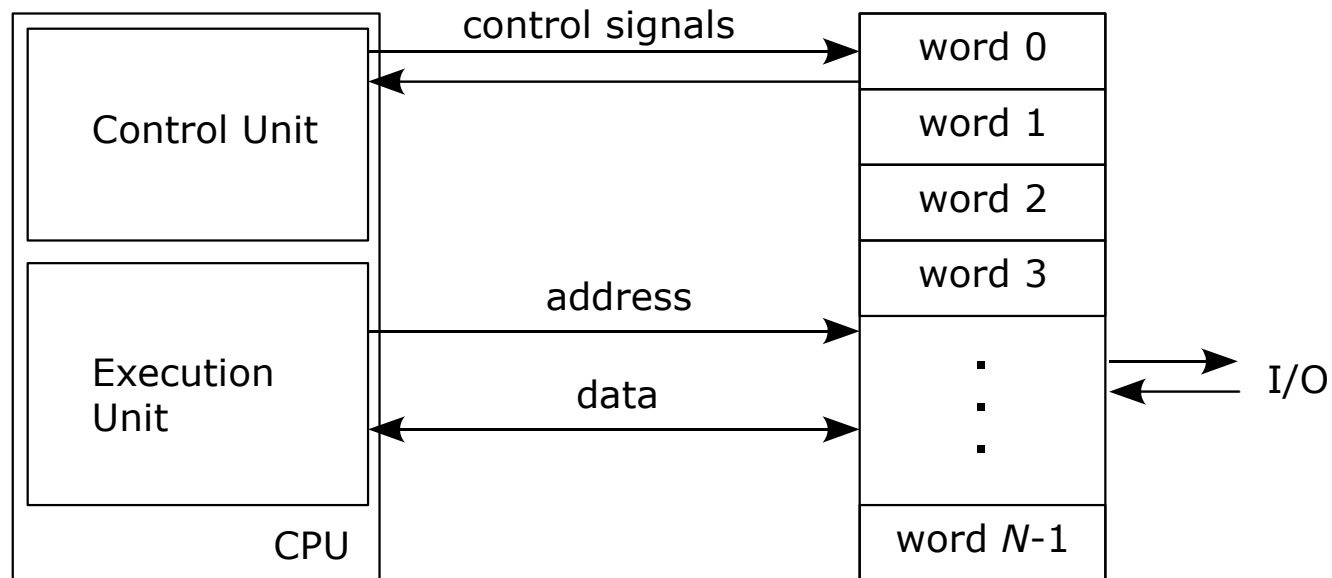


Architecture and components of Computer System

# Models of Computer Systems

The stored program concept (1945) - program instructions are stored, as well as data, in computer read-write memory.

The von Neumann architecture (e.g. PC Intel architecture computers)



Memory organisation:

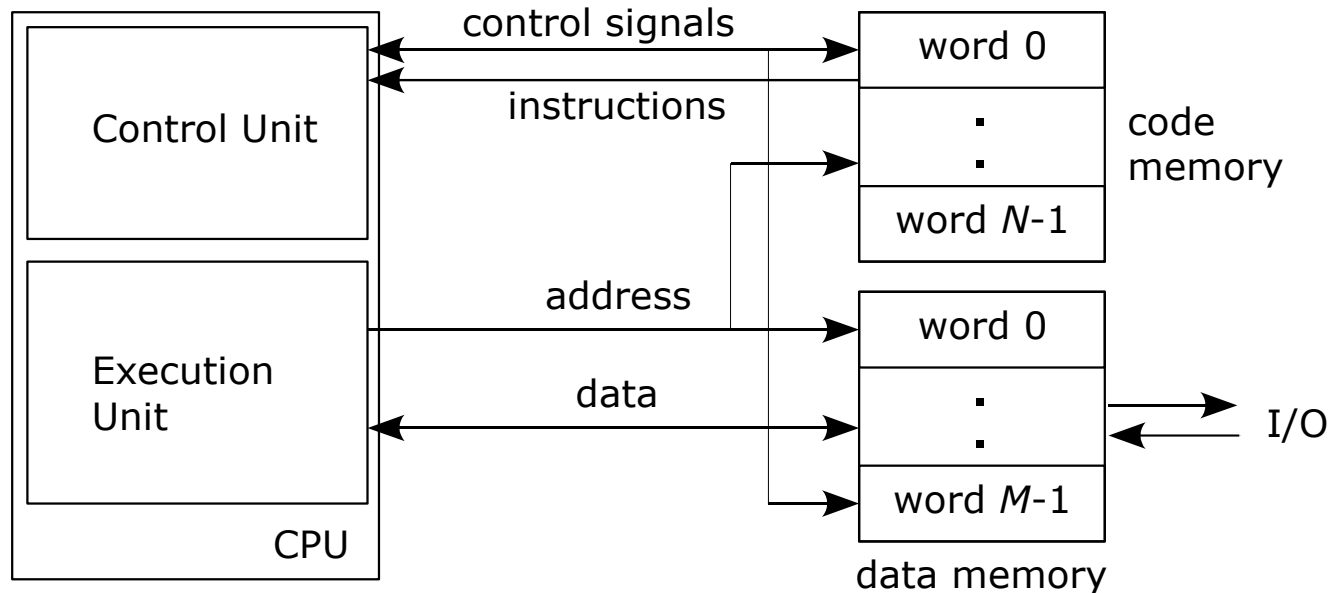
- code and data are stored in cells (words) of constant width,
- both code and data are stored in the same way,
- interpretation of word (code or data) depends on current context,
- each memory cell is identified by unique address,
- instructions and data cannot be read at the same time because they use the same bus system (disadvantage).

Architecture and components of Computer System

# Models of Computer Systems

The Harvard architecture (1948 r.) (e.g. DSPs, PIC Microchip Tech. microcontrollers)

In this architecture data and code memories are physically separated.



Advantages of code and data separation:

- the Harvard architecture computer can be faster for the given circuit complexity,
- code is protected against accidental destruction.

Architecture and components of Computer System

# Data And Code Representation

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In modern computers code and data are stored as numbers represented in binary numeral system. Such representation is convenient for digital electronic circuits.

## Binary numeral system

This is the numeral system with a radix of 2.

$$num_{(10)} = \sum_{i=0}^{N-1} b_i 2^i = b_{N-1} 2^{N-1} + b_{N-2} 2^{N-2} + \dots + b_1 2^1 + b_0 2^0,$$

where  $b_i \in \{0, 1\}$ .

Example:

$$119_{(10)} = 1110111_{(2)}, \quad 55632_{(10)} = 1101100101010000_{(2)}, \quad 4342_{(10)} = 1000011110110_{(2)}.$$

Digits  $b_i$  are called *bits*.

8 bits (b) → 1 byte (B), 1024 bytes → 1 kB, 1024 kB → 1 MB, 1024 MB → 1 GB.

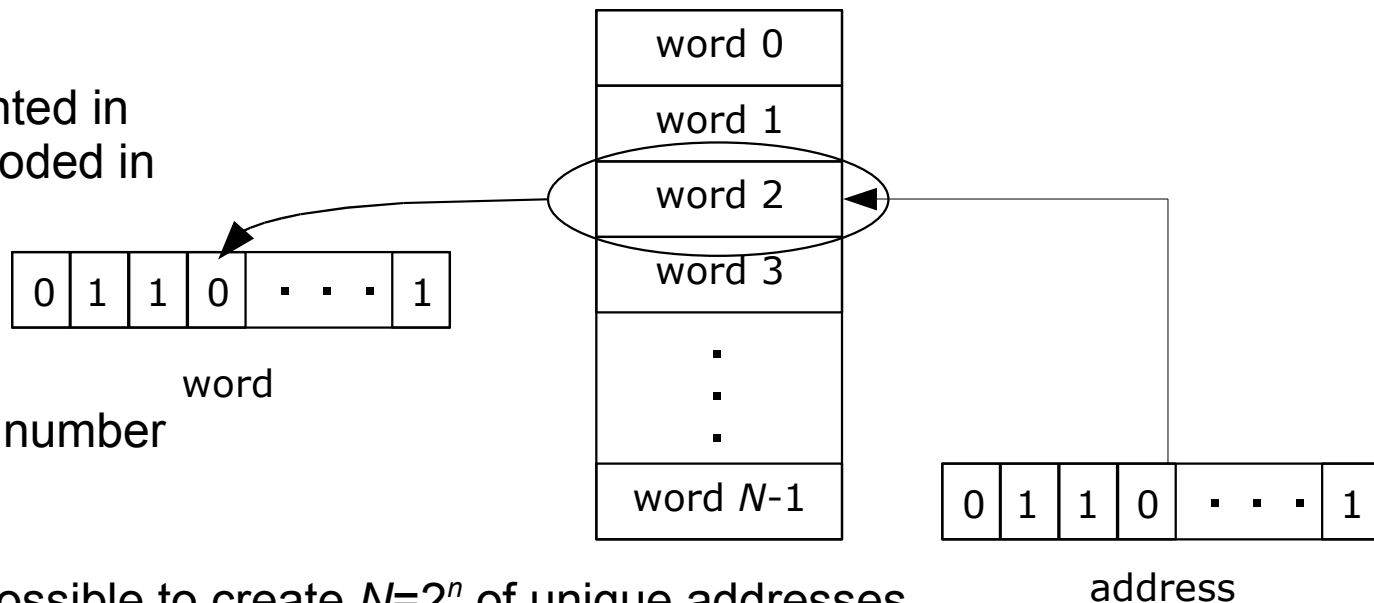
Word depending on specific architecture can be:

- 8 bits (8-bit architecture),
- 16 bits (16-bit architecture),
- 32 bits (32-bit architecture),
- 64 bits (64-bit architecture) long.

# Data And Code Representation

## Representation in memory:

Data and code are represented in memory cells as numbers coded in binary system.

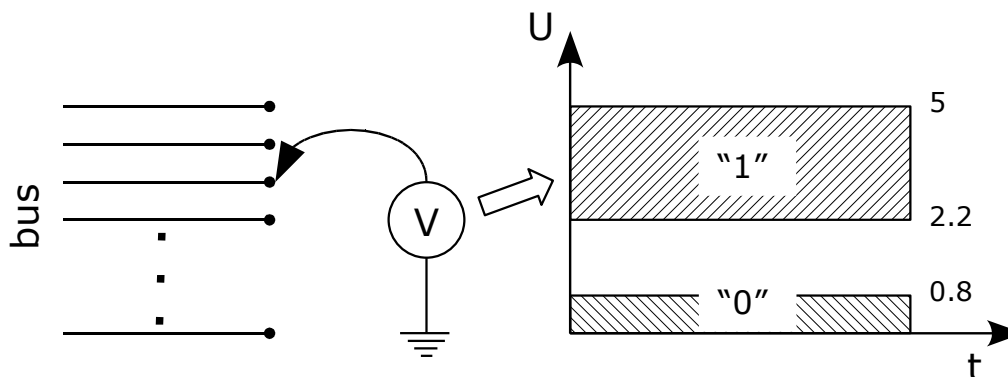


The cell's address is also a number in binary system.

In  $n$ -bit binary system it is possible to create  $N=2^n$  of unique addresses and hence up to  $N$  different memory cells can be addressed.

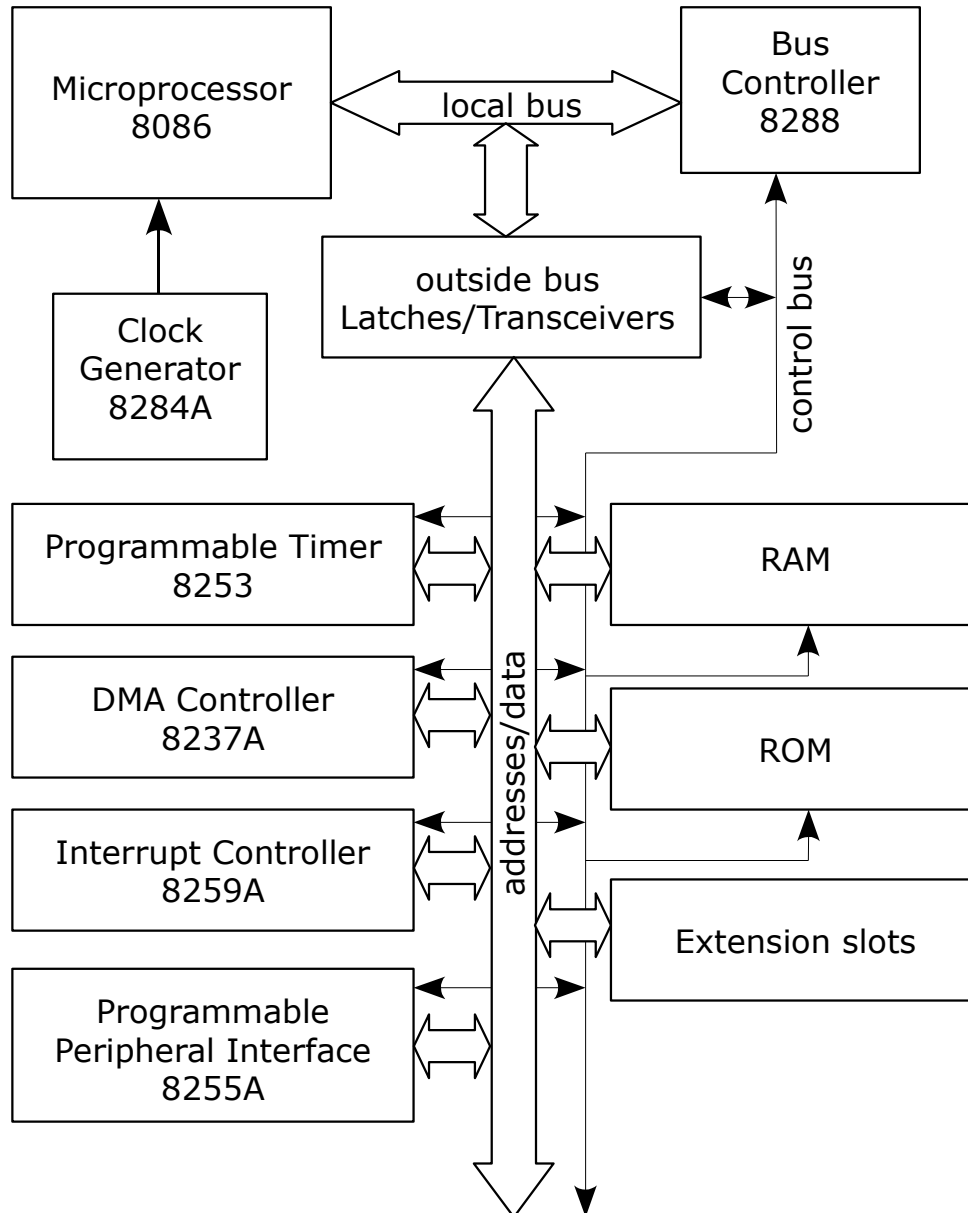
Buses (control, data and code bus) are  $n$ -bit wide and enable information flow, i.e. control, data and code signals, between all elements of computer systems.

In electronic implementation binary information is coded in shape of electric signals. Binary "0" and "1" are represented as signals of specific voltage ranges.



# PC XT Architecture

The block diagram of PC/XT architecture computer:

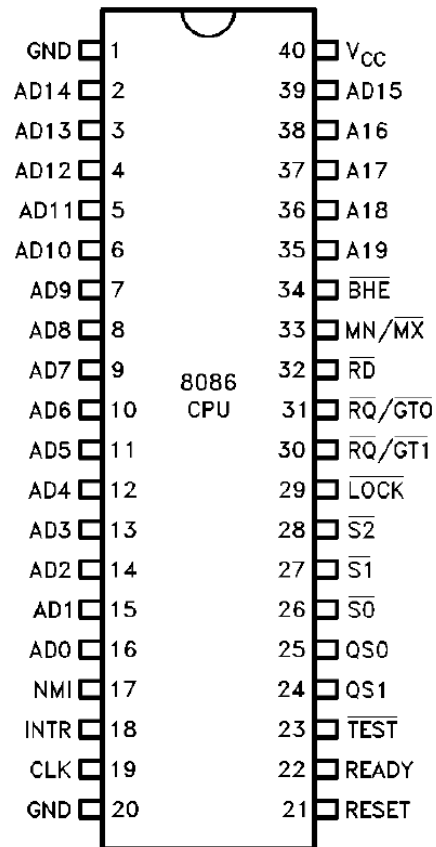


Clock Generator (8284A) - generates the system clock: 5MHz or 8MHz;  
Bus Controller (8288) - supports  $\mu$ P by generating control signals;  
Latches (8282) - retain addresses and control signals;  
Transceivers (8286) - act as bidirectional latches for data signals;  
Progr. Timer (8253) - contains three 16-bit counters for: system clock, DRAM memory refreshing signals, sound generator;  
DMA Contr. (8237A) - executes fast memory to memory data transfer;  
Interrupt Contr. (8259A) - collects and prioritises requests from peripheral devices  
Progr. Peripheral Interface (8255A) - plays a role of interfacing device to: keyboard, FDD printer, CRT, etc. drivers;  
RAM - read/write memory: code/data storage;  
ROM - read only memory: BIOS;  
Ext. slots - enable system extension with other devices: graphic, sound cards, etc.

# PC XT Architecture

The heart of PC/XT architecture constitutes the Intel 8086 16-bit microprocessor.

## Pin description for 8086 microprocessor:



AD<sub>15</sub> - AD<sub>0</sub>: multiplexed address/data bus lines;

A<sub>16</sub> - A<sub>19</sub>: remaining address bus lines;

BHE: bus high enable, enables data onto most significant 8 bits of data bus;

S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub>: status used by 8288 bus controller to generate all memory and I/O access control signals:

S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	
0	0	0	- Interrupt Acknowledge,
0	0	1	- Read I/O Port,
0	1	0	- Write I/O Port,
1	0	1	- Read Memory,
1	1	0	- Write Memory;

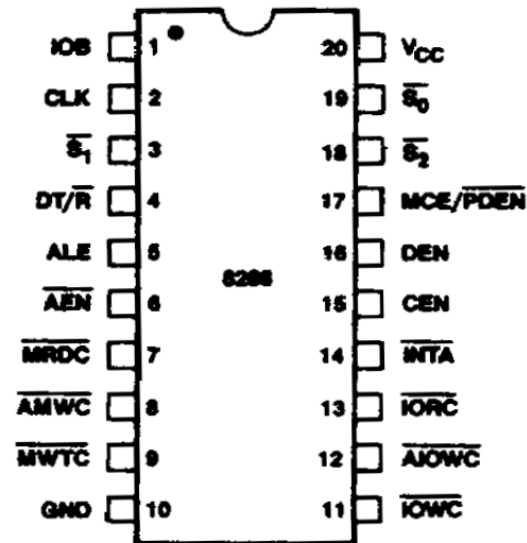
CLK: clock line that provides basic timing for the processor and bus controller;

RESET: causes the processor to immediately terminate its current activity and restart;

READY: is the acknowledgement from memory or I/O device that data transfer is completed.

# PC XT Architecture

## Pin description for 8288 Bus Controller:



$\overline{MRDC}$ : memory read demand;

$\overline{MWTC}$ : memory write demand;

$\overline{IORC}$ : I/O device read demand;

$\overline{IOWC}$ : I/O device write demand;

INTA: interrupt acknowledge signal;

CLK: system clock input;

DEN: signal for data bus transceiver to keep current state of the bus;

ALE: signal for address and control buses latches to keep current state;

DT/ $\overline{R}$ : indicates data direction of data transfer (to or from memory, I/O device);

$\overline{S}_0$ ,  $\overline{S}_1$ ,  $\overline{S}_2$ : status signals from 8086 microprocessor;

# PC XT Architecture

Typical configuration of 8086 microprocessor (working in maximum mode):

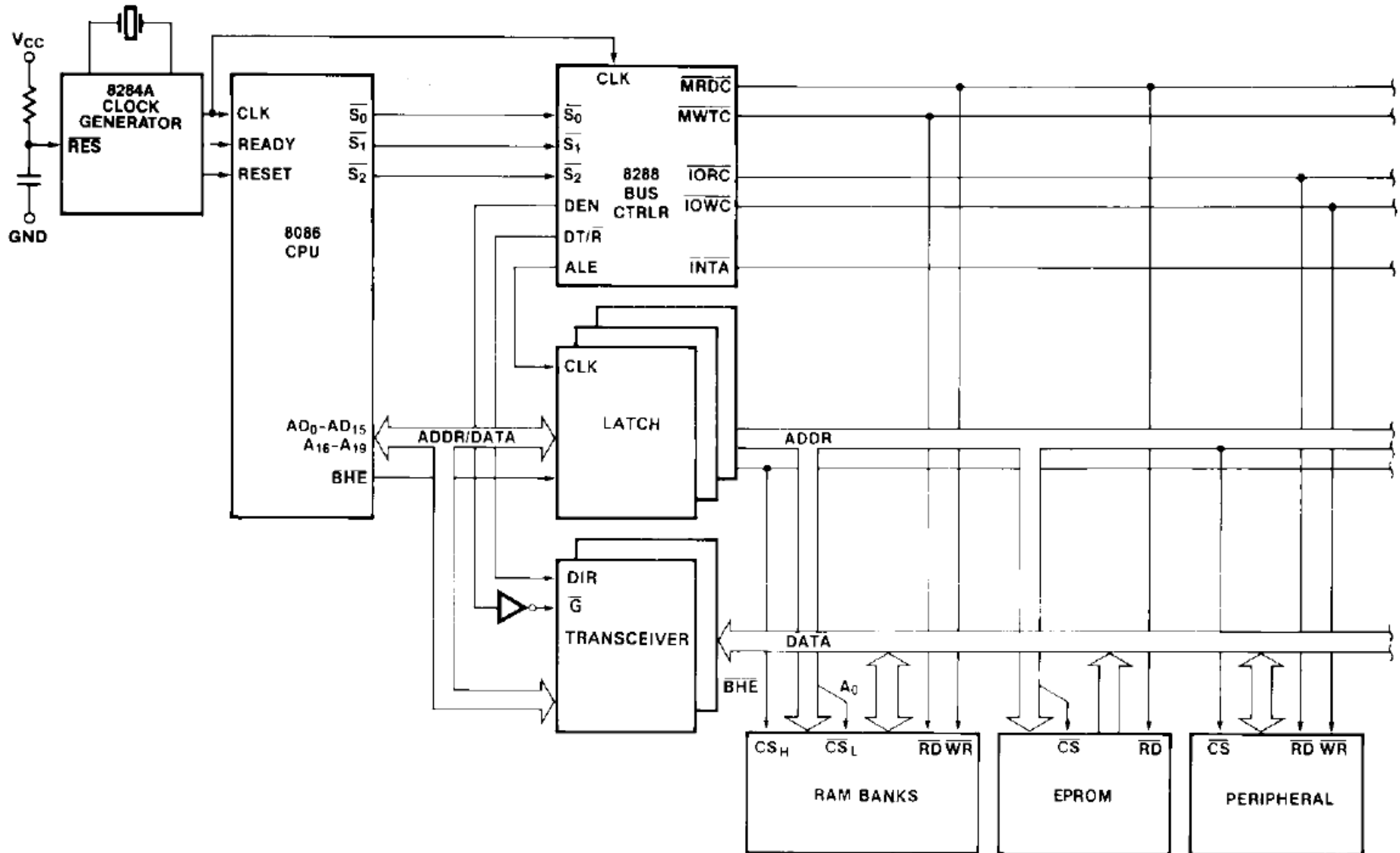


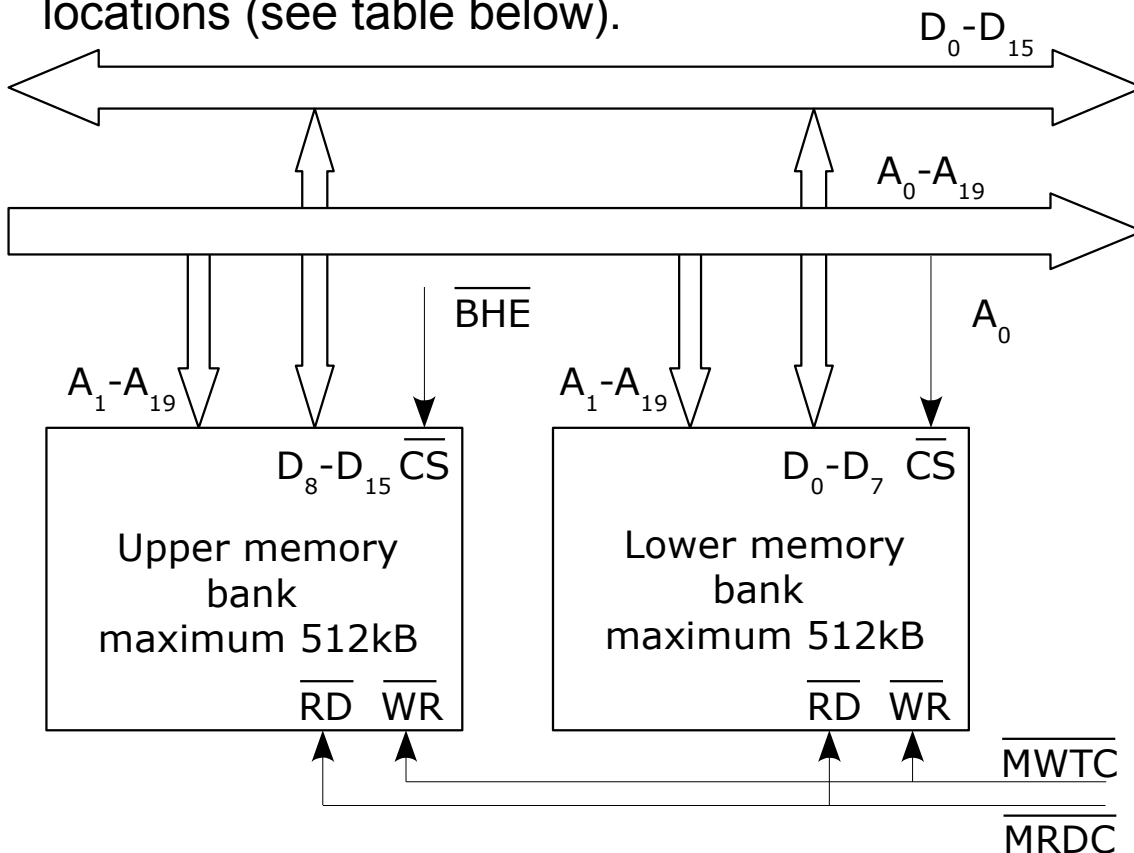
Image source: Intel manual



# PC XT Architecture

## Memory organization:

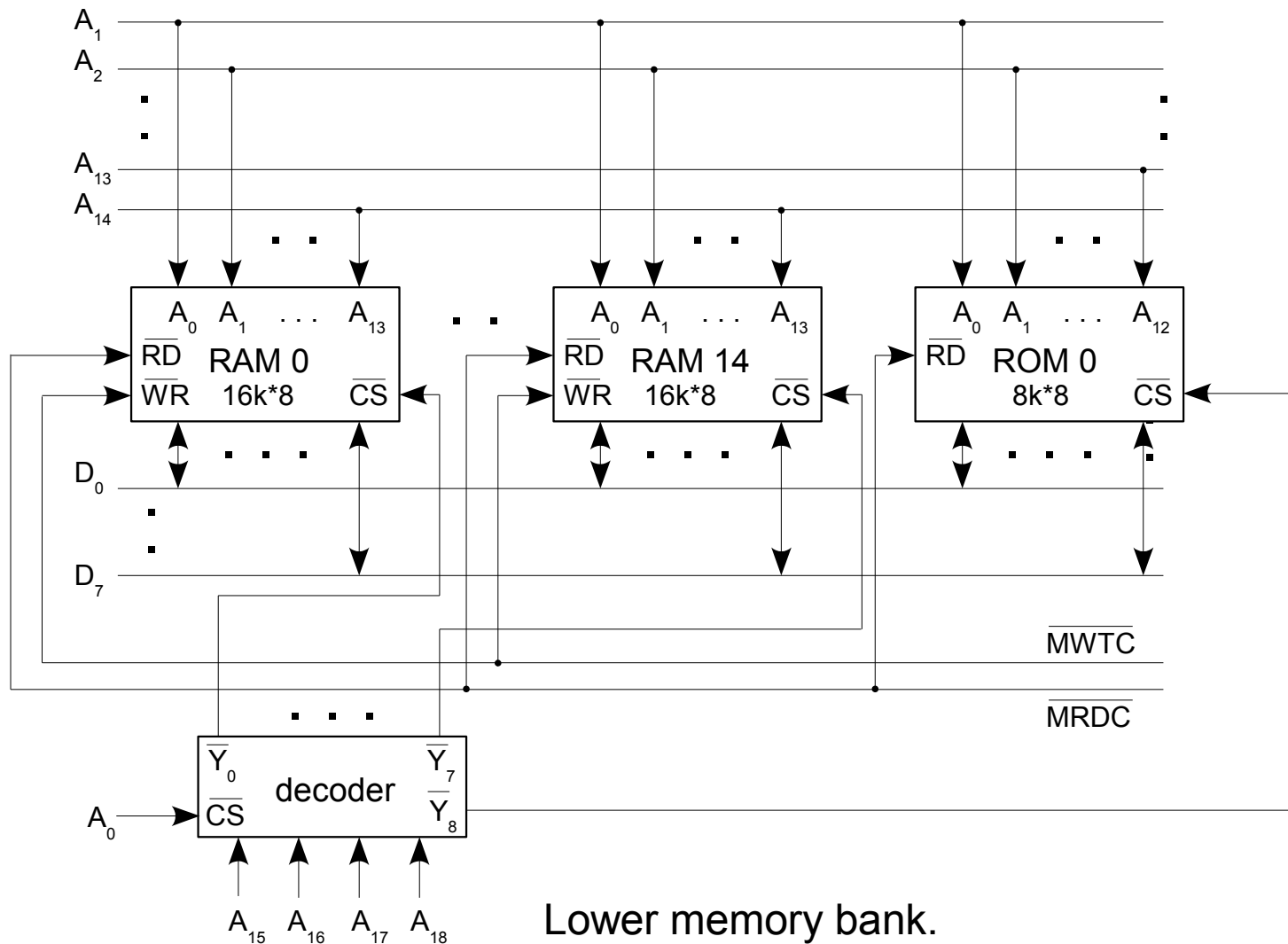
Physically memory is organised in high ( $D_8-D_{15}$ ) and low ( $D_0-D_7$ ) order blocks each up to 512k of 8-bit memory. Byte data with even addresses is transferred on  $D_0-D_7$  lines while odd addressed data is transferred on lines  $D_8-D_{15}$ . The processor and Bus Controller provide  $\overline{\text{BHE}}$  and  $A_0$  lines for selective reading or writing into either odd or even byte locations (see table below).



$\overline{\text{BHE}}$	$A_0$	Characteristics
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

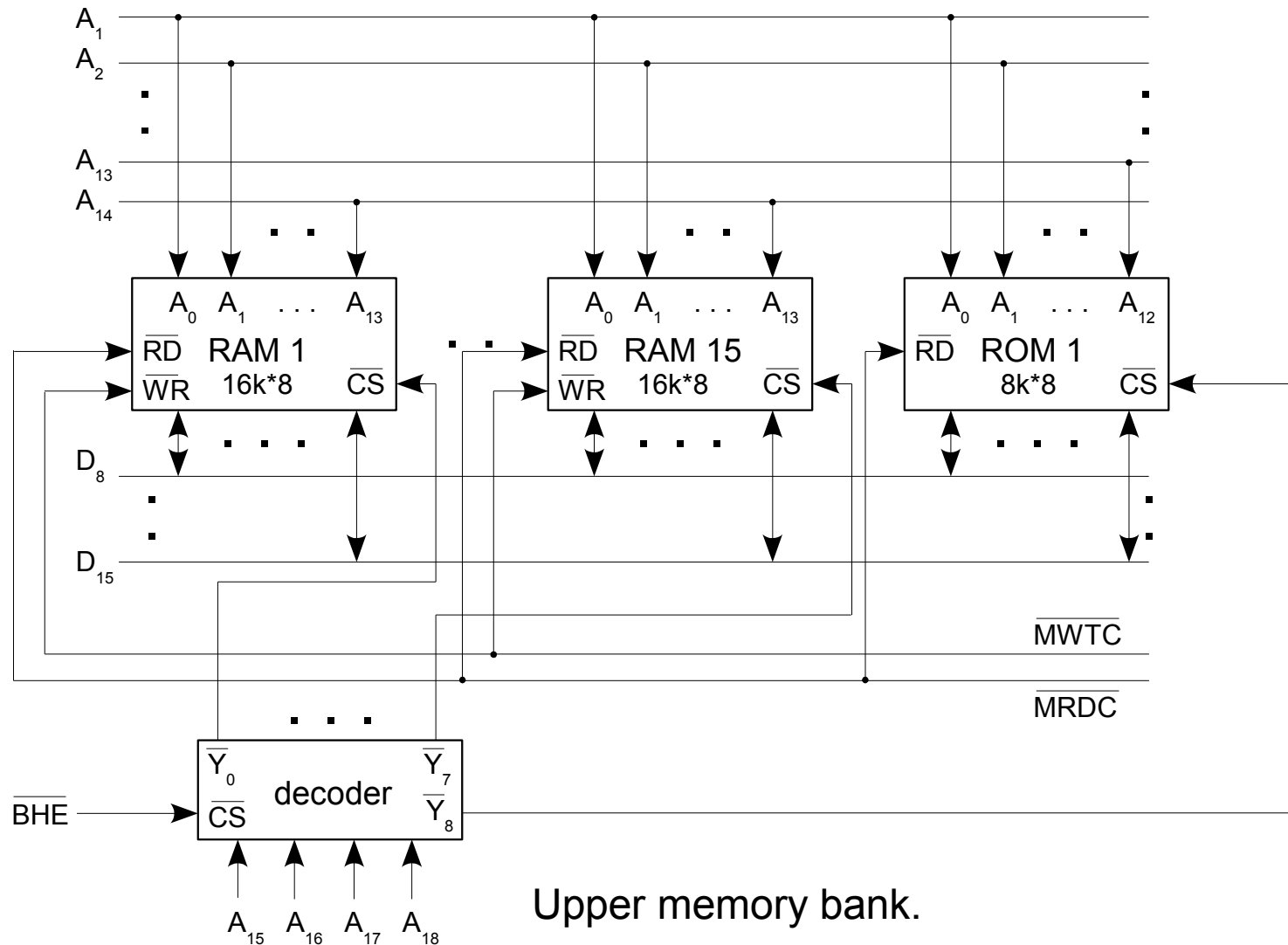
# PC XT Architecture

Exemplary memory configuration:



# PC XT Architecture

## Exemplary memory configuration:



# PC XT Architecture

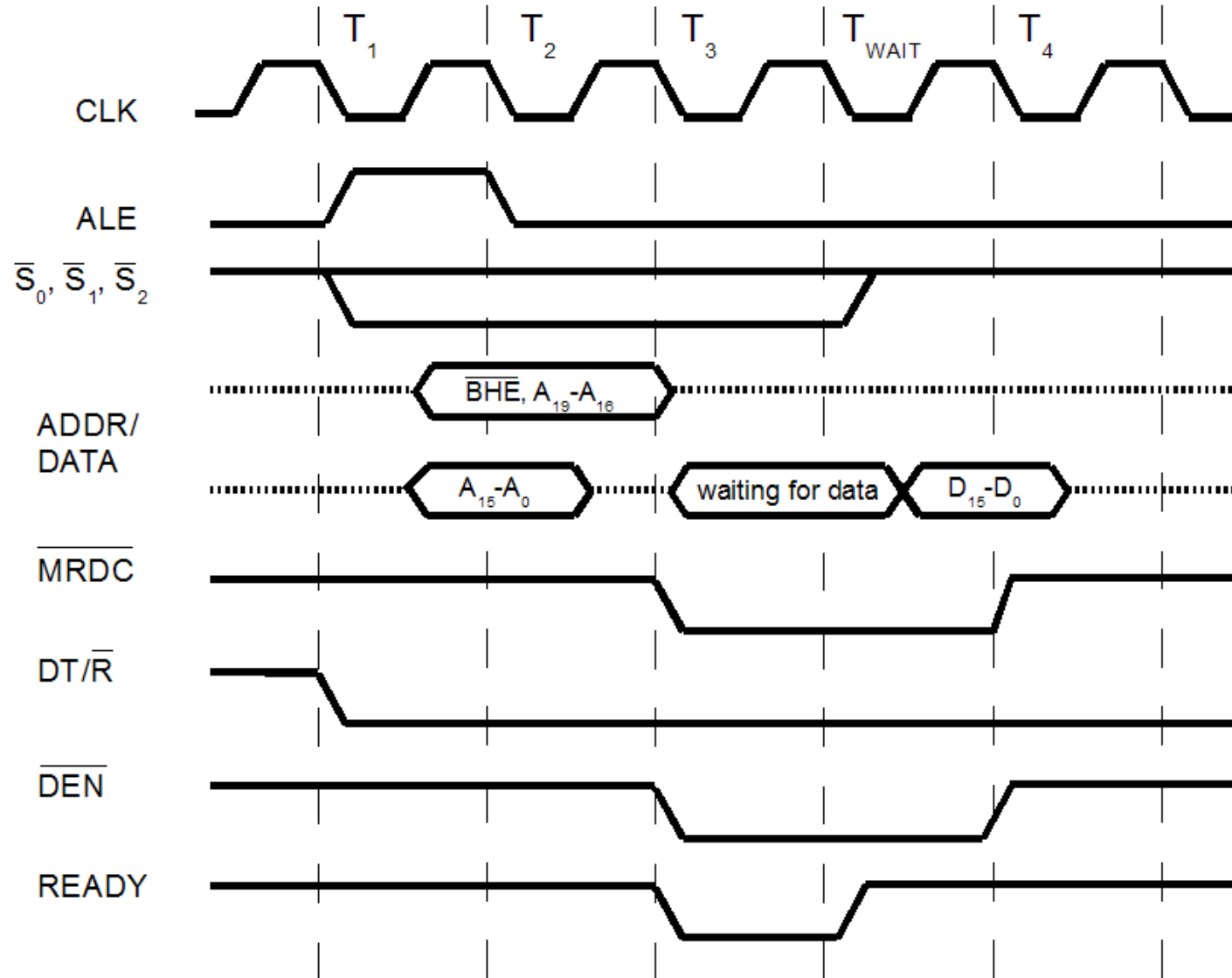
## Memory map:

Chips	A <sub>19</sub>	A <sub>18</sub>	A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>	A <sub>11</sub>	A <sub>10</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>
RAM 0 and 1	x x	0 0	0 0	0 0	0 0	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1
RAM 2 and 3	x x	0 0	0 0	0 0	1 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1
RAM 4 and 5	x x	0 0	0 0	1 1	0 0	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1
RAM 6 and 7	x x	0 0	0 0	1 1	1 1	as above														
RAM 8 and 9	x x	0 0	1 1	0 0	0 0	as above														
RAM 10 and 11	x x	0 0	1 1	0 0	1 1	as above														
RAM 12 and 13	x x	0 0	1 1	1 1	0 0	as above														
RAM 14 and 15	x x	0 0	1 1	1 1	1 1	as above														
ROM 0 and 1	x x	1 1	0 0	0 0	0 0	x x	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1

Size of available Random Access Memory - 256 kB,  
Size of available Read Only Memory - 16 kB.

# PC XT Architecture

Memory read operation timings:



# PC XT Architecture

Memory write operation timings:

